

ABSTRACT

Controllers for power electronic converters are commonly developed through a sequence of simulation-based environments of increasing realism. In controller hardware-in-the-loop (CHIL) testing, the final validation stage before connection to the physical converter, the controller executes in real time against a simulated plant. However, the simulator interacts with the controller only through its external inputs and outputs, limiting visibility to the controller boundary at precisely the stage where timing, synchronization, and hardware-related defects first become observable. This dissertation argues that the limitation arises from the location of the simulator interface rather than from real-time execution itself and introduces the CHILplug, a grey-box CHIL methodology that relocates the interface from the controller boundary to selected boundaries within its control-layer hierarchy.

The CHILplug redirects signals crossing internal control-layer boundaries through a network-based interface, allowing selected controller states to participate in and be observed during a real-time experiment. Depending on the selected boundary, the same architecture supports conventional CHIL, partial CHIL in which only selected control layers execute on hardware, and monitoring of internal controller states during testing or operation. Because the interface resides within the controller, it remains available throughout the equipment lifecycle and can be used after commissioning without requiring duplicate hardware or modifications to the installed system.

The methodology is demonstrated on a medium-voltage switched-capacitor modular multilevel converter (SC-MMC) controller implemented on a commercial platform. A CHILplug based on an Aurora 8B/10B communication link was used throughout controller development and commissioning, enabling incremental validation of control layers, diagnosis of defects inaccessible through terminal measurements alone, and comparison of simulated and measured behavior under identical operating conditions.

To formalize the design process, a four-step methodology is developed and expressed as a binary integer linear program. Using only a set of test modes, controller signals, and candidate communication interfaces, the formulation determines the minimum CHILplug architecture that satisfies communication and timing constraints. Applied retrospectively to the deployed controller, the methodology reproduces the implemented architecture and identifies the same communication limitations encountered during development.