ABSTRACT

Many embedded systems are introducing processing units to accelerate the processing speed of tasks, such as for multi-media applications. The units are mostly customized designs. Another method of designing accelerator is using pre-defined standard intellectual properties. However, the procedure of arranging IP cores in a system and maintaining a high performance as well is challenging. Implementing softcore processors on field-programmable gate arrays (FPGAs) is a relatively fast and inexpensive choice to design and validate a desired system. This thesis describes the rapid prototyping of hardware/software co-design based on FPGAs. A novel system generator to effortlessly design a multiple NIOS II soft-processor core systems is also proposed. The NIOS II CPU is a configurable RISC processor designed by Altera/Intel and can be customized to complete specific tasks. The error-prone and time-consuming process of designing an IP block-based system is improved by the new novel system generator. The detail of the implementation of such system is discussed. To test the performance of a multi-NIOS II system, a parallel application is executed on 1-, 2-, 5-, and 10-core NIOS II systems separately. Test results prove the feasibility of the proposed methodology, a FIR filter is used as testing application. The demonstration systems of FIR filter show improvement of 29% for dual-core system compared to single core system, improvement of 28% a 5-core system compared to the dual-core system. Furthermore, image processing algorithms were implemented on the expanded 1-, 2-, 4-, 8-core Nios II systems. Power consumption and temperature of the board were monitored. For the thresholding algorithm, a 2-core system is 15.11% faster than a 1-core system. A 4-core system is 31.0639 % faster than a 2-core system. An 8-core system is 40.2503% faster than a 4-core system.